Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) An apparatus, comprising:

two or more memories having one or more redundant components associated with each memory, the one or more redundant components include at least one redundant column of memory cells;

a first processor containing redundancy allocation logic to execute one or more repair algorithms to generate a repair signature for each of the two or more memory; and

a repair data container to store an actual repair signature for each memory having one or more defective memory cells detected during fault testing and a dummy repair signature for each memory with no defective memory cells.

2. (Original) The apparatus of claim 1, wherein the repair data container storing the repair signature for each memory is a fuse box located external to a memory block.

3. (Original) The apparatus of claim 1, wherein the dummy repair signature for each memory with no defect is an identifier bit directing the processor to bypass loading of reconfiguration data into the memory corresponding to this identifier bit.

4. (Original) The apparatus of claim 1, wherein the dummy repair signature for each memory with no defect is an identifier bit directing the processor to load a pre-stored series of reconfiguration data bits into scan chain registers of the memory corresponding to this identifier bit but the content of the reconfiguration data bits does not cause a substitution of a redundant component for a non-redundant component in that memory.

5. (Currently Amended) The apparatus of claim ~~1~~2, wherein the fuse box contains one or more fuses and a fuse is a non-volatile storage device that performs the function of a fuse.

6. (Original) The apparatus of claim 1, wherein the processor further includes logic configured to compress an amount of bits making up the actual repair signature.

7. (Currently Amended) The apparatus of claim ~~1~~6, wherein the processor further includes logic configured to decompress an amount of bits making up the actual repair signature.

8. (Original) The apparatus of claim 1, wherein the processor further includes logic configured to compose a concatenated repair signature for all of the memories sharing a fuse box.

9. (Original) The apparatus of claim 1, wherein the repair data container contains an amount of fuses to store actual repair signatures for an adjustable subset of the redundant components associated with the two or more memories and dummy repair signatures for the remaining memories.

10. (Original) The apparatus of claim 1, wherein the repair data container stores indicator bits for each memory sharing that repair data container, and a presence of an active bit in the indicator bits indicates that the repair data container contains an actual repair signature for that memory having a defect.

11. (Original) The apparatus of claim 2, wherein the fuse box has a dedicated field for each memory sharing that fuse box, and a presence of an active bit in the dedicated field indicates that the fuse box contains an actual repair signature for that memory having a defect.

12. (Original) The apparatus of claim 1, wherein the processor further includes logic configured to provide built in self-test logic, built-in self-diagnosis logic, and reconfiguration data logic.

13. (Original) The apparatus of claim 1, further comprises:

compression/decompression logic around the repair data container configured to compress an amount of bits making up a repair signature and decompress an amount of bits making up a repair signature.

14. (Original) The apparatus of claim 1, wherein the processor, repair data container, and the memories are embedded on a single chip.

15. (Currently Amended) The apparatus of claim 1, further comprising:

two or more processors including the processor as a first processor and a second processor wherein thea second processor ~~containing~~contains redundancy allocation logic and is coupled to one or more memories, wherein the repair data container to store a concatenated repair signature that repairs the memories connected the first processor as well as the memories connected to the second processor.

16. (Currently Amended) An apparatus, comprising:

a repair data container located on a chip, the repair data container to store an actual repair signature for each memory having a defective memory cell; ~~and~~

two or more memories located on the chip, each memory having redundant components that share the repair data container, wherein the repair data container has an amount of fuses to store the actual repair signatures for an adjustable subset of the two or more memories; and

a processor, located on the chip, having logic configured to test the memories during each cycle of operation and to generate an augmented repair signature if a new defect is detected.

17. (Original) The apparatus of claim 16, wherein the repair data container also stores dummy repair signatures for each memory with no defective memory cells.

18. (Currently Amended) The apparatus of claim 17, ~~further comprising:~~ wherein thea processor also containscontaining redundancy allocation logic and is coupled to the repair data container, wherein the repair data container ~~to~~ stores a concatenated repair signature that includes the actual repair signatures and the dummy repair signatures.

19. (Currently Amended) The apparatus of claim 17, further comprising: wherein thea ~~first~~ processor coupled is to the repair data container~~, wherein~~ and the ~~first~~ processor contains logic configured to decompress an amount of bits making up the actual repair signatures.

20. (Canceled)

21. (Currently Amended) The apparatus of claim 19, further comprising: two or more processors including the processor as a first processor and a second processor wherein thea second processor containing logic configured to test and repair memories connected to the second processor; wherein the repair data container has an amount of fuses to store the actual repair signatures for an adjustable subset of the memories connected to the second processor as well as memories connected to the first processor.

22. (Original) An apparatus, comprising:

a first processor containing logic configured to test and repair two or more memories connected to that first processor;

a second processor containing logic configured to test and repair two or more memories connected to that second processor; and

a fuse box to store a concatenated repair signature that repairs the memories connected the first processor as well as the memories connected to the second processor.

23. (Original) The apparatus of claim 22, wherein the first processor contains logic configured to decompress an amount of bits making up the concatenated repair signature.

24. (Original) The apparatus of claim 22, further comprising:

an amount of non-volatile fuses contained in the fuse box to provide actual repair capability for only a subset of all of the memories that share the fuse box.

25. (Original) The apparatus of claim 22, wherein the fuse box is located external to the memories.

26. (Currently Amended) The apparatus of claim ~~1~~22, wherein the processors and the fuse box are embedded on a single chip.

27. (Currently Amended) A method, comprising:

composing a repair signature for two or more ~~memories~~memory cores on every cycle a device containing the two or more memory cores is initialized;

sending the repair signature for each memory core to be stored in non-volatile fuses; and

decompressing the repair signature for each memory core to send reconfiguration data to the two or more ~~memories~~memory cores.

28. (Currently Amended) The method of claim of 27, further comprising:

storing an actual repair signature for a subset of the two or more ~~memories~~memory cores and a dummy repair signature for the remaining ~~memories~~memory cores.

29. (Currently Amended) The method of claim of 27, further comprising:

repairing an adjustable subset of ~~memories~~memory cores having redundant elements.

30. (Currently Amended) An apparatus, comprising:

means for composing a repair signature for two or more ~~memories~~memory cores on every cycle a device containing the two or more memory cores is initialized;

means for sending the repair signature for each memory core to be stored in non-volatile fuses; and

means for decompressing the repair signature for each memory core to send reconfiguration data to the two or more ~~memories~~memory cores.

31. (Currently Amended) The apparatus of claim of 30, further comprising:

means for storing an actual repair signature for a subset of the two or more ~~memories~~memory cores and a dummy repair signature for the remaining ~~memories~~memory cores.

32. (Currently Amended) The apparatus of claim of 30, further comprising:

means for repairing an adjustable subset of ~~memories~~memory cores having redundant elements.

33. (Currently Amended) A machine readable medium that stores data and executable instructions representing an integrated circuit, which when executed by a machine to cause the machine to generate a representation of the integrated circuit including~~comprising~~:

a first processor containing logic configured to test and repair two or more memories connected to that first processor;

a second processor containing logic configured to test and repair two or more memories connected to that second processor; and

a fuse box to store a concatenated repair signature that repairs the memories connected the first processor as well as the memories connected to the second processor.

34. (Currently Amended) The machine-readable medium of claim ~~32~~33, wherein the machine-readable medium comprises a memory compiler to provide a layout utilized to generate one or more lithographic masks used in the fabrication of the fuse box and the processors.

35. (Currently Amended) A machine readable medium that stores data and executable instructions representing an integrated circuit, which when executed by a machine to cause the machine to generate a representation of the integrated circuit including~~comprising~~:

a repair data container located on a chip, the repair data container to store an actual repair signature for each memory core having a defect; and

two or more ~~memories~~memory cores having redundant components that share the repair data container, wherein the repair data container has an amount of fuses to store the actual repair signatures for an adjustable subset of the two or more ~~memories~~memory cores; and

a processor having logic configured to test the ~~memories~~memory cores during each cycle of operation and to generate an augmented repair signature if a new defect is detected.

36. (Currently Amended) The machine-readable medium of claim 35, wherein the machine-readable medium comprises a memory compiler to provide a layout utilized

to generate one or more lithographic masks used in the fabrication of the repair data container and the two or more ~~memories~~memory cores.

37. (Currently Amended) A machine readable medium that stores data and executable instructions representing an integrated circuit, which when executed by a machine to cause the machine to generate a representation of the integrated circuit including~~comprising~~:

two or more memories having one or more redundant components associated with each memory, the one or more redundant components include at least one redundant column of memory cells;

a processor containing redundancy allocation logic to execute one or more repair algorithms to generate a repair signature for each memory; and

a repair data container to store an actual repair signature for each memory having one or more defective memory cells and a dummy repair signature for each memory with no defective memory cells.

38. (Currently Amended) The machine-readable medium of claim 37, wherein the machine-readable medium comprises a memory compiler to provide a layout utilized to generate one or more lithographic masks used in the fabrication of the repair data container, the processor, and the two or more memories.